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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: KIYOSHI DEMIZU ET AL

Serial No.: Not Yet Assigned Group Art Unit:

Filed: December 27, 2001 Examiner:

CAM#: 29368.029

Title: SEMICONDUCTOR WAFER AND DEVICE SEMICONDUCTOR DEVICE MANUFACTURING PROCESS

PRELIMINARY AMENDMENT

Box PCT
To the Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

Preliminary to examination of the above-captioned PCT national stage application, kindly amend the application as follows:

In the claims:

Please cancel claims 1 through 16, inclusive, without prejudice or disclaimer and substitute therefor the following new claims 17 through 35:

17. (New) A semiconductor wafer having a roughness of the backside surface varied in a direction of a radius, wherein varied sections exist substantially coaxially in the direction of the radius.

18. (New) A semiconductor wafer having a roughness of the backside surface varied in a direction of a radius, wherein sections of the different

roughness exist at least in a peripheral part of the wafer and in a arbitrary sections inner than the periphery.

19. (New) A semiconductor wafer according to claim 1, wherein the variation of the roughness of the backside surface in the direction of the radius is continuous in the direction of the radius.

20. (New) A semiconductor wafer according to claim 1, wherein the variation of the roughness of the backside surface in the direction of the radius is stepwise so that the roughness varies with each approximately designated annular width in the radius direction.

21. (New) A semiconductor wafer according to claim 1, wherein a roughness wavelength of the coarser section in the roughness of the wafer backside surface is within the range of 5 to 100 μ m.

22. (New) A semiconductor wafer, which is held on a wafer holding means by a face to face contact of the whole backside surface, having a contact surface density forming means of the backside surface thereof, the contact surface density forming means prepared so as to vary in a direction of a radius to have a varying contact surface density distribution in the direction of the radius with respect to the contact surface density of the backside of the wafer to the wafer holding means.

23. (New) A semiconductor wafer according to claim 6, wherein the contact surface density forming means is a surface roughness distribution varied in the direction of the radius.

24. (New) A method for processing a semiconductor wafer comprising steps of polishing the backside of a wafer and providing a surface roughness of the back side of the wafer varying substantially coaxially in a direction of a radius by at least one process means selected from process means except for polishing process.

25. (New) A method for processing a semiconductor wafer according to claim 8, wherein at least one process means is etching or surface grinding.

26. (New) A method for processing a semiconductor wafer comprising steps of forming a oxide film on a backside of a wafer, removing the oxide film partially by etching, removing the residual oxide film by polishing the whole area of the backside, whereby providing coaxially a roughness distribution approximately in a direction of a radius.

27. (New) A method for processing a semiconductor wafer according to claim 10, wherein the partial removal of the oxide film by etching comprises inserting tightly the wafer coaxially between two disk like pads of corrosion-resistant material having a diameter smaller than a diameter of the wafer and removing the oxide film of the exposed part like an annular rim by etching.

28. (New) A method for processing a semiconductor wafer according to claim 10, wherein the partial removal of the oxide film by etching comprises inserting tightly the wafer coaxially between two annular rim like pads of corrosion-resistant material having an outer diameter equal to or larger than a diameter of the wafer and an inner diameter smaller than the diameter of the wafer and removing the oxide film of the exposed disk like part by etching.

29. (New) In an apparatus of process for fabricating semiconductor devices wherein a whole backside surface of a wafer is held by a wafer holding means by face to face contact to carry out device fabricating processes thereon, an apparatus of process for fabricating semiconductor devices comprising a means for adjusting a contact surface density at least on a surface of the wafer holding means, the backside of the wafer or a means for applying contact pressure between both surfaces so as to have varying contact surface densities between the wafer and the surface of the wafer holding means in a direction of the wafer diameter.

30. (New) An apparatus of process for fabricating semiconductor devices according to claim 13, wherein the adjustment of the contact surface density of the surface of the wafer holing means is done by giving nearly coaxially a roughness distribution in a direction of a radius of the wafer.

31. (New) An apparatus of process for fabricating semiconductor devices

according to claim 14, wherein the roughness distribution is given by forming a gathering of annular recesses, dotted recesses or the combination thereof on the center or outer part of the surface of the wafer holding means to contact the wafer surface.

32. (New) An apparatus of process for fabricating semiconductor devices according to claim 13, wherein the means for applying contact pressure between the wafer holding means and the backside of the wafer is a means for adjusting the electrostatic charge of an electrostatic chuck.

33. (New) A semiconductor wafer according to claim 2, wherein the variation of the roughness of the backside surface in the direction of the radius is continuous in the direction of the radius.

34. (New) A semiconductor wafer according to claim 2, wherein the variation of the roughness of the backside surface in the direction of the radius is stepwise so that the roughness varies with each approximately designated annular width in the radius direction.

35. (New) A semiconductor wafer according to claim 2, wherein a roughness wavelength of the coarser section in the roughness of the wafer backside surface is within the range of 5 to 100 μ m.

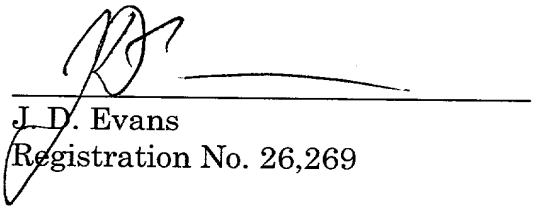
REMARKS

The foregoing amendments are respectfully submitted to replace the international-style claims of the original PCT text with claims in better form for examination by the U.S. Patent and Trademark Office.

Entry of the amendments and favorable action on the application are earnestly solicited.

Respectfully submitted,

December 27, 2001



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